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R Graham

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Paylor
5-16-02

In re Application of

Chen et al.

Serial No.: 09/748,256 / Group Art Unit: 2811 /

Filed: December 27, 2000 / Examiner: Ori Nadav /

For: METHOD FOR FABRICATING COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) DEVICES ON A MIXED BULK AND SILICON-ON-INSULATOR (SOI) SUBSTRATE

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231
Box AF

AMENDMENT UNDER 37 C.F.R. §1.116

Sir:

In response to the Office Action dated April 22, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims to read as follows:

29. (Twice Amended) A semiconductor device comprising:

a bulk silicon region comprising single crystal silicon; and

a silicon-on-insulator (SOI) region comprising:

an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon; and

at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

41. (Thrice Amended) A hybrid bulk silicon and silicon-on-insulator (SOI) substrate,